	Annii antian Na	Applicant/a	
	Application No.	Applicant(s)	
Al-41 All L.1114	10/015,209	HASHIMOTO, EIKI	( Ph)
Notice of Allowability	Examiner	Art Unit	
	A. M. Thompson	2825	
The MAILING DATE of this communication appear All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in or other appropriate commu IGHTS. This application is s	this application. If not included nication will be mailed in due cour	se. <b>THIS</b>
1. This communication is responsive to <u>04 April 2005 - 12 Ma</u>	a <u>y 2005</u> .		
2.   The allowed claim(s) is/are 2, 4, 5, 7, 9, 10, 14, 16, 18, 19,	renumbered (37 CFR 1.126	<u>)</u> .	
3. The drawings filed on 16 November 2001 and 17 June 200	<u>04</u> are accepted by the Exam	iner.	,
<ul> <li>4.  Acknowledgment is made of a claim for foreign priority unerstanding a)  All b)  Some* c)  None of the:</li> <li>1.  Certified copies of the priority documents have</li> </ul>	, •	or (f).	
2. Certified copies of the priority documents have	e been received in Application	n No	
3. Copies of the certified copies of the priority do	cuments have been received	in this national stage application	from the
International Bureau (PCT Rule 17.2(a)).			
* Certified copies not received:			
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		a reply complying with the require	ments
5. A SUBSTITUTE OATH OR DECLARATION must be subminformal PATENT APPLICATION (PTO-152) which give			CE OF
6. CORRECTED DRAWINGS (as "replacement sheets") mus	st be submitted.		
(a) ☐ including changes required by the Notice of Draftspers		(PTO-948) attached	
1)  hereto or 2)  to Paper No./Mail Date			
(b) including changes required by the attached Examiner's Paper No./Mail Date		in the Office action of	
Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in t			k) of
7. DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT			the
•			
Attachment(s)		•	
1. Notice of References Cited (PTO-892)	5. Notice of Inf	ormal Patent Application (PTO-15	2)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)		mmary (PTO-413),	
3. Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 05/12/05;04/04/05	Paper No.// 08), 7. ☐ Examiner's /	Mail Date Amendment/Comment	
4.   Examiner's Comment Regarding Requirement for Deposit	8. 🗌 Examiner's S	Statement of Reasons for Allowan	ce
of Biological Material	9.	A. M. Thompson	
		Primary Examiner Technology Center 2800 (	

## **DETAILED ACTION**

Applicants' amendment to 10/015,209 has been examined and remarks reviewed. Claims 1, 3, 6, 8, 11-13, 15, 17 and 20 are cancelled. Claims 14 is amended. Claims 2, 4, 5, 7, 9, 10, 14, 16, 18, and 19 are pending.

1. Applicants' amendment coupled with the instant Examiner's amendment places this application in a condition for allowance. Claims 2, 4, 5, 7, 9, 10, 14, 16, 18, and 19 are herein allowed.

## **EXAMINER'S AMENDMENT**

2. An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Brian E. Hennessey, 51,271 on or about 21 June 2005.

The application has been amended as follows:

3. **Replace** Claim 14 with the following:

A semiconductor circuit designing method, comprising:

(a) providing an inspection item database section in which a circuit feature of a semiconductor integrated circuit for which a logical design should be executed corresponds to an inspection item of an inspection to be executed before a layout design of said semiconductor integrated circuit is executed;

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(b) notifying a circuit designer executing said logical design of said

semiconductor integrated circuit of said inspection item, retrieved from said inspection

item database section;

(c) executing said logical design of said semiconductor integrated circuit

by said circuit designer with reference to said inspection item; and

(d) executing said layout design of said semiconductor integrated circuit

by a layout designer with respect to said inspection item.

Conclusion

4. Any inquiry concerning this communication or earlier communications should be

directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The

Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

5. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop \_\_\_\_\_

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

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or faxed to:

(703) 872-9306, (for all OFFICIAL communications intended for entry)

A. M. THOMPSON
Primary Examiner
Technology Center 2800